

PTO-1449 REPRODUCED				ATTORNEY DOCKET NO. 2789.2011-001		APPLICATION NO.	
INFORMATION DISCLOSURE CITATION IN AN APPLICATION May 16, 2001 (Use several sheets if necessary)				APPLICANT Ramin Farjad-Rad			
				FILING DATE		GROUP	
U.S. PATENT DOCUMENTS							
EXAM- INER INI- TIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE IF APPROPRIATE
	AA						
	AB						
	AC						
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION YES NO
	AL						
	AM						
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							
	AR	Lee, Thomas H., et al., "A 155-MHZ Clock Recovery Delay - and Phase-Locked Loop," pp. 421-430, Reprinted from IEEE Journal of Solid-State Circuits, vol. SC-27, pp. 1736-1746, December 1992.					
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	AT	Savoj, Jafar, et al., "A 10-Gb/s CMOS Clock and Data Recovery Circuit," IEEE, pp. 136-139.					
	AU	Poulton, John, et al., "A Tracking Clock Recovery Receiver for 4Gb/s Signaling," pp. 157-169.					
	AV	Hu, Timothy H., "A Monolithic 480 Mb/s Parallel AGC/Decision/Clock-Recovery Circuit in 1.2- μ m CMOS," pp. 437-443, Reprinted from IEEE Journal of Solid-State Circuits, vol. SC-28, pp. 1314-1320, December 1993.					
	AW	Ishihara, Noboru, et al., "A Monolithic 156 Mb/s Clock and Data Recovery PLL Circuit Using the Sample-and-Hold Technique," pp. 431-436, Reprinted from IEEE Journal of Solid-State Circuits, vol. SC-29, pp. 1566-1571, December 1994.					
	AX	Farjad-Rad, Ramin, et al., "A 0.3- μ m CMOS 8-Gb/s 4-PAM Serial Link Transceiver," pp. 757-764, May 2000					
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EXAMINER Ard Kulkarni				DATE CONSIDERED 9/25/02			

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